REMARKS

Claims 1-5, 21 and 22 are pending in this case. Claims 1 and 22 are amended with this response. Applicant notes with appreciation that the request for reexamination has been accepted and the submission filed. Reconsideration of the application in light of the following remarks is respectfully requested.

I. REJECTION OF CLAIM 22 UNDER 35 U.S.C. § 112

Claim 22 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claim 22 has been amended to clarify two "wherein" clause areas identified by the examiner. These areas will also be discussed further in section II below. Accordingly, withdrawal of the indefiniteness rejection is respectfully requested.

II. REJECTION OF CLAIMS 1-5, 21 and 22 UNDER 35 U.S.C. § 103(a)

Claims 1-5, 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moise et al. U.S. Patent No. 6,211,035 (hereinafter, Moise) in view of Fox et al. U.S. Patent No. 6,627,930 (hereinafter, Fox).

Claims 1-5 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchiyama et al. US Patent No. 6,831, 313 (Uchiyama) in view of Fox et al. U.S. Patent No. 6,627,930 (hereinafter, Fox). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to recite *an integrated circuit, comprising an array of ferroelectric memory cells, each cell having a capacitor stack having an upper electrode, a lower electrode, and a single ferroelectric core layer with a crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack. At least one of the capacitor stacks comprises* ***a conductive contact formed under the capacitor stack*** *wherein* ***the conductive contact has a cross section near a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric cores****.*

Applicant respectfully submits that amended independent claim 1 is patentable over Moise in view of Fox as the references do not teach or suggest capacitor stacks each having an upper electrode, a lower electrode, and a single ferroelectric core layer, wherein at least one of the capacitor stacks comprises a conductive contact formed under the capacitor stack and wherein the conductive contact has **a cross section near a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric cores**. By contrast, Moise illustrates in the Fig. 10b and 10d, for example, a lower contact plug 1020 that appears to be substantially smaller than that of the ferroelectric capacitor cores 1024/1026. Similarly, lower contact plug 320 of Figs. 6c and 6f of Moise appears to be substantially smaller than the overlying ferroelectric capacitors 624/626. The same discussion and conclusion also applies to Uchiyama, which has a contact 120 that does not have a cross-section near a contact portion with the bottom portion of the capacitor stack 128 that is about as large or larger than that of the ferroelectric cores 124. According to one non-limiting aspect of the present invention, the metal plugs filling the vias in the dielectric layer over (and/or under) the ferroelectric cores is equal or greater to that of the ferroelectric cores in order to add to the thermal stresses that help reorient the domains during cooling (ref. page 5 lines 24-27 and page 7 lines 7-11). Fox is not applied to teach the underlying conductive contact. Accordingly, Applicant respectfully submits that claim 1 and the claims which depend therefrom are patentable over the references.

Claim 22 has been amended to recite *an integrated circuit,…wherein at least one of the capacitor stacks comprises* ***a first conductive contact formed over the capacitor stack****, and* ***a second conductive contact formed under the capacitor stack****.* ***The first and second conductive contacts each have a cross section near a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric cores****.*

Similarly, the applicant respectfully submits that amended independent claim 22 is patentable over Moise in view of Fox as the references do not teach or suggest capacitor stacks each having an upper electrode, a lower electrode, and a single ferroelectric core layer, wherein at least one of the capacitor stacks comprises ***a first***

conductive contact formed over the capacitor stack**, and **a second conductive contact formed under the capacitor stack wherein both *the **first and second conductive contacts each have a cross section near a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric cores**.*

Again, by contrast, Moise illustrates in the Fig. 10b and 10d, for example, a lower contact plug 1020 that appears to be substantially smaller than that of the ferroelectric capacitor cores 1024/1026. Similarly, lower contact plug 320 of Figs. 6c and 6f of Moise appears to be substantially smaller and than the overlying ferroelectric capacitors 624/626. The same discussion and conclusion also applies to Uchiyama, which has a contact 120 that does not have a cross-section near a contact portion with the bottom portion of the capacitor stack 128 that is about as large or larger than that of the ferroelectric cores 124. According to one non-limiting aspect of the present invention, the metal plugs filling the vias in the dielectric layer over (and/or under) the ferroelectric cores is equal or greater to that of the ferroelectric cores in order to add to the thermal stresses that help reorient the domains during cooling (ref. page 5 lines 24-27 and page 7 lines 7-11). Again, Fox is not applied to teach the underlying conductive contact. Accordingly, Applicant respectfully submits that claim 22 and the claims which depend therefrom are patentable over the references.

In addition, Fox et al. do not teach a **single ferroelectric core layer,** as recited in claims 1 and 22. By contrast, Fox et al. teach **a multi-layered** crystallographic textured structure, wherein the multiple "textures" describe multiple "crystal planes" (column 1, lines 60-61 of Fox et al.) of multiple ferroelectric layers, or a *first ferroelectric layer having a first crystallographic texture and a second ferroelectric layer having a second differing crystallographic texture* (Abstract, lines 6-10 of Fox et al.), and therefore the cited art does not teach this feature of the claimed invention.

In addition, Fox et al. teach against the **single ferroelectric core layer** structure of claims 1 and 22 of the present invention, for example, stating that *the **multi-layered ferroelectric capacitors** disclosed provide much enhanced performance and operating characteristics over conventional ferroelectric devices incorporating dielectric layers having **but a single crystallographic texture*** (a single Fe-layer) (Column 2, lines 59-

63 of Fox et al.). Thus, one would not be motivated to combine the teaching of Fox et al. teaching ***multiple ferroelectric layers*** with Uchiyama et al. teaching a ***single homogenous ferroelectric core*** (Column 2, lines 18-22 of Uchiyama et al.) because such a modification would render the structure of Fox et al. unsatisfactory for it's intended purpose.

Fox et al. also teach against the **single ferroelectric core layer** structure of claims 1 and 22 of the present invention, for example, teaching that *the* ***use of the added ferroelectric layer 24*** significantly reduces the undesired effects of dipole "pinning" which might otherwise occur when the bottom or top electrodes 12, 14 directly adjoin the ferroelectric bulk (core) (Column 2, lines 37-40 of Fox et al.). Thus, one would not be motivated to combine the above teachings of Fox et al. with Uchiyama et al. teaching a ***single homogenous ferroelectric core*** *material*, or a ***single composite material*** *comprising a ferroelectric component and a dielectric component* (Abstract, lines 3-6, and Column 2, lines 18-22 of Uchiyama et al.)

Finally, Fox et al. discourage the <001> ***crystallization family*** orientation recited in claims 1 and 22, stating that growing ***ferroelectric dielectric layers having a <001> crystallographic texture*** *is generally* ***more difficult than growing*** *<111> or RND material,* which *is generally utilized* (Column 4, lines 17-21 of Fox et al.).

As highlighted above, the primary reference, Moise et al., do not teach the invention of independent claims 1 or 22, and one of ordinary skill in the art would not be motivated to combine with Fox et al. or be motivated to modify the reference in accordance with Uchiyama et al. Therefore claims 2-5 and 21 are believed to be non-obvious over the cited art, and withdrawal of the rejections is therefore respectfully requested.

III. CONCLUSION

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36398.

Respectfully submitted,
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